Appl. No. 09/545,785

IN THE CLAIMS

1. (Currently Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction and lying in a first plane, the first plane disposed above a substrate;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying in a second plane above the first plane, each of the second level lines being disposed over a respective one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four coplanar line pairs, each line pair comprising one of the first level lines and a respective one of the second level lines, the coplanar line pairs being substantially parallel to, and extending vertically upward from the substrate;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of vias arranged in a plurality of groups, each group corresponding uniquely to one of the coplanar line pairs and each group including at least two vias connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four vertically oriented parallel capacitor plates , the vertically oriented parallel plates being spaced apart from each other, and only dielectric material being disposed between each of the vertically oriented parallel plates; and

electrically opposing nodes forming the terminals of the capacitor, the array of vertically oriented parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the vertically oriented parallel capacitor plates have alternating electrical polarities;

**wherein each vertically oriented parallel capacitor plate comprises a mesh structure**.

2. (Original) The capacitor of claim 1, wherein the conductive lines comprise metal.

3. (Original) The capacitor of claim 1, wherein the conductive lines comprise polysilicon.

4. (Original) The capacitor of claim 1, wherein the dielectric layer comprises silicon dioxide.

5. (Previously Presented) The capacitor of claim 1, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying in a third plane above the first and second planes such that each of the third level lines is coplanar with a respective one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

so that the third lev l of lin s vertically xtends the array of at least four parallel capacitor plates.

6. (Previously Presented) The capacitor of claim 1, wherein the first and the at least second multiple levels of electrically conductive parallel lines comprise a plurality of electrically conductive parallel lines arranged in vertical plates, and the dielectric layer comprises a plurality of dielectric layers, each of the layers disposed between opposing levels of conductive lines.

7. (Cancelled)

8. (Currently Amended) The capacitor of claim 1 ~~7~~, wherein the substrate is made from a semiconductor material.

9. (Original) The capacitor of claim 1, wherein the capacitor comprises a sub-micron MOS structure.

10. (Cancelled)

11. (Original) The capacitor of claim 1, wherein the capacitor comprises a sub-micron structure.

12. (Previously Present d) The capacitor of claim 1, wher in each resp ctive plurality of vias of the at least four line pairs of the at least four parallel capacitor plates is arranged opposite a next said respective plurality of vias, with identical spacing of vias in each plurality of vias.

13. (Currently Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction above a substrate;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying above the first level, each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four line pairs, each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

a dielectric layer disposed between the first and second levels of conductive lines;

a plurality of groups of vias, each group corresponding to one of the line pairs and each group including a plurality of vias directly connecting the first level line and the second level line of the corresponding line pair, thereby forming an array of at least four parallel vertically oriented ~~screen~~ **mesh** structures, each ~~screen~~ **mesh** structure having dielectric filled openings therein and only the dielectric is disposed between the vertically oriented ~~screen~~ **mesh** structures; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel vertically oriented ~~screen~~ **mesh** structures electrically connected to the opposing nodes in an alternating manner so that the vertically oriented ~~screen~~ **mesh** structures have alternating electrical polarities.

14. (Currently Amended) The capacitor of claim 13, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between the second and third levels of conductive lines,

wherein the third level of lines vertically extends the array of at least four parallel vertically oriented ~~screen~~ **mesh** structures.

15. (Previously Presented) The capacitor of claim 13, wherein the vias in each group are identically spaced apart.

16. (Previously Presented) The capacitor of claim 13, wherein each group includes four vias.

17. (Previously Presented) The capacitor of claim 13, wherein each group includes:

a first via directly connecting the first level line and the second level line of the corresponding line pair at respective first ends of the first and second level lines; and

a second via directly connecting the first level line and the second level line of the corresponding line pair at respective second ends of the first and second level lines,

wherein the second ends are opposite the first ends along the first direction.

18. (Currently Amended) A capacitor comprising:

a first level of at least four electrically conductive parallel lines extending in a first direction;

at least a second level of at least four electrically conductive parallel lines extending in the first direction and lying above the first level, each of the second level lines being disposed over a corresponding one of the first level lines, such that the lines of the first and second levels are arranged in a series of at least four line pairs, each line pair comprising one of the first level lines and the corresponding one of the second level lines disposed thereover;

a dielectric layer disposed between portions of the first and second levels of conductive lines, disposed on the first level adjacent the parallel lines of the first level, and further disposed on the second level adjacent the parallel lines of the second level;

a plurality of groups of vias, each group including a plurality of vias extending directly between the first level line and the second level line of a line pair, thereby forming an array of at least four parallel capacitor plate structures, the plate structures being spaced apart from each other, and only the dielectric being disposed between each of the plate structures; and

electrically opposing nodes forming the terminals of the capacitor, the array of parallel capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities;

**wherein each parallel capacitor plate structure comprises a mesh structure**.

19. (Previously Presented) The capacitor of claim 18, further comprising:

at least a third level of electrically conductive parallel lines extending in the first direction and lying above the first and second levels such that each of the third level lines is disposed over a corresponding one of said line pairs; and

a second dielectric layer disposed between portions of the second and third levels of conductive lines ,disposed on the third level adjacent the parallel lines of the third level,

wherein the third level of lines vertically extends the array of at least four parallel capacitor plate structures.

20. (Previously Presented) The capacitor of claim 18, wherein each group includes four vias.

21. (Currently Amended) The capacitor of Claim 19, wherein each of the at least four plate structures ~~form a screen with the~~ **have** dielectric disposed in the openings of the **mesh** ~~screen~~, the plate structures extend vertically upward from a substrate and are perpendicular to the substrate.